IN THE SPECIFICATION:

Please replace the paragraph at page 16, lines 15-27, as follows:

The first gate-gate electrode layer 20 is formed in a manner to pass between the first p^+-type impurity layer 14a and the second p^+-type impurity layer 14b, in the first active region 14. In other words, the first gate-gate electrode layer 20, the first p^+-type impurity layer 14a and the second p^+-type impurity layer 14b form the first load transistor Q5. Also, the first gate-gate electrode layer 20 is formed in a manner to pass between the second n^+-type impurity layer [16a] 16b and the third n^+-type impurity layer 16c, in the third active region 16. In other words, the first gate-gate electrode layer 20, the second n^+-type impurity layer [16a] 16b and the third n^+-type impurity layer 16c form the first driver transistor Q3.